ESR

HCAL Front-end Electronics Report

December, 2002

Theresa Shaw

FE Electronics Documentation

CCA and QIE specifications

http://www-ppd.fnal.gov/tshaw.myweb/CMS_ASIC_new.htm

Backplane specifications

http://www-ppd.fnal.gov/tshaw.myweb/CMS_Backplane.html

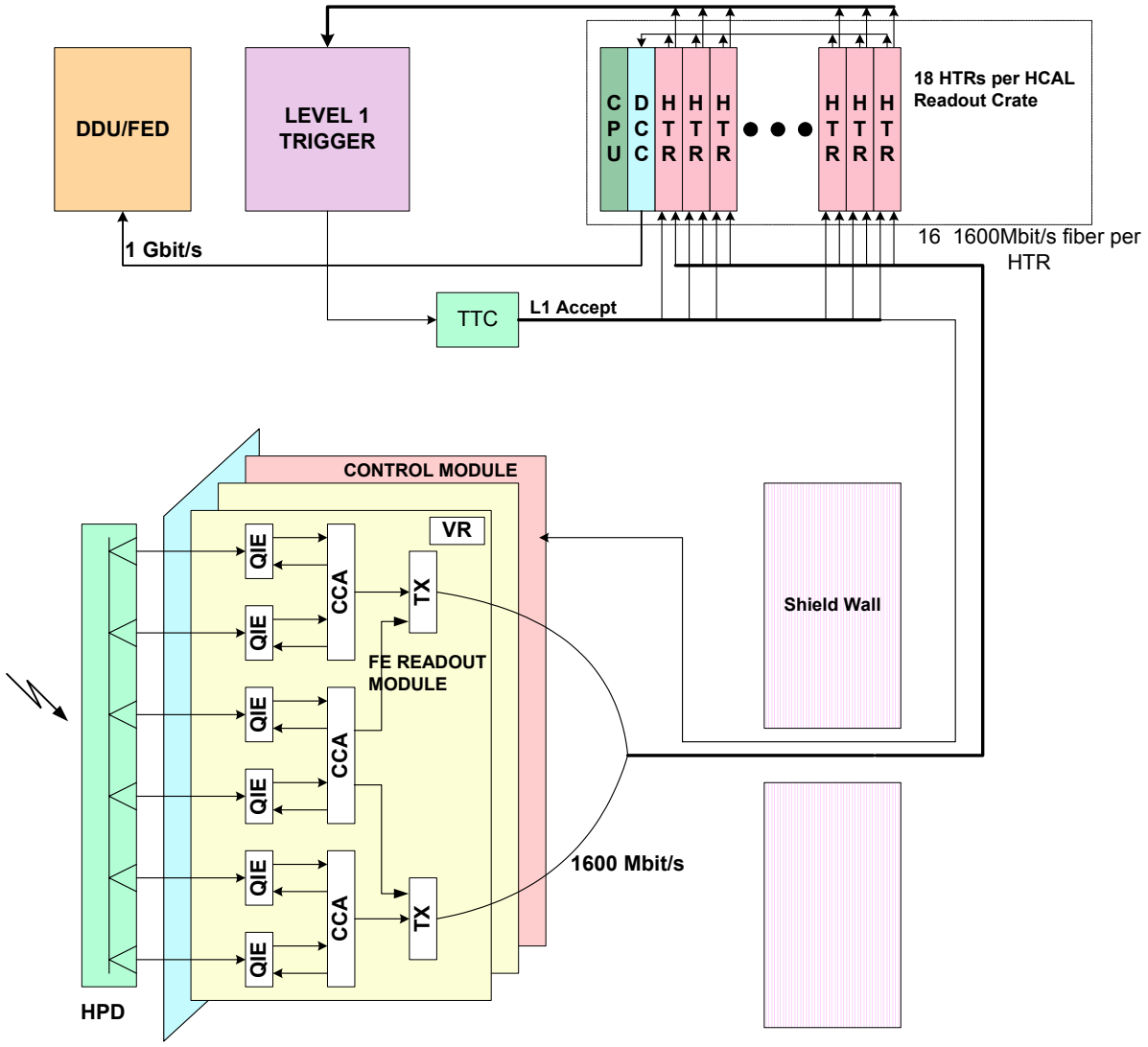
Front End Module specification

http://www-ppd.fnal.gov/tshaw.myweb/CMS_Design.html

Clock and Control Module documents

http://www-ppd.fnal.gov/holm.myweb/CMS_HCAL.htm

FE/DAQ Electronics



Front End Electronics

Principal components:

1. **QIE (charge integrator and encoder)**
   Fermilab ASIC
2. **CCA (channel control ASIC)**
   Fermilab ASIC
3. **GOL (gigabit optical link)**
   CERN ASIC
4. **L4913 (rad hard voltage regulator)**
   STC ASIC from CERN specifications
5. **HFE419X-521 (connectorized VCSEL diode)**
   Honeywell standard 2.5 Gbit/sec device

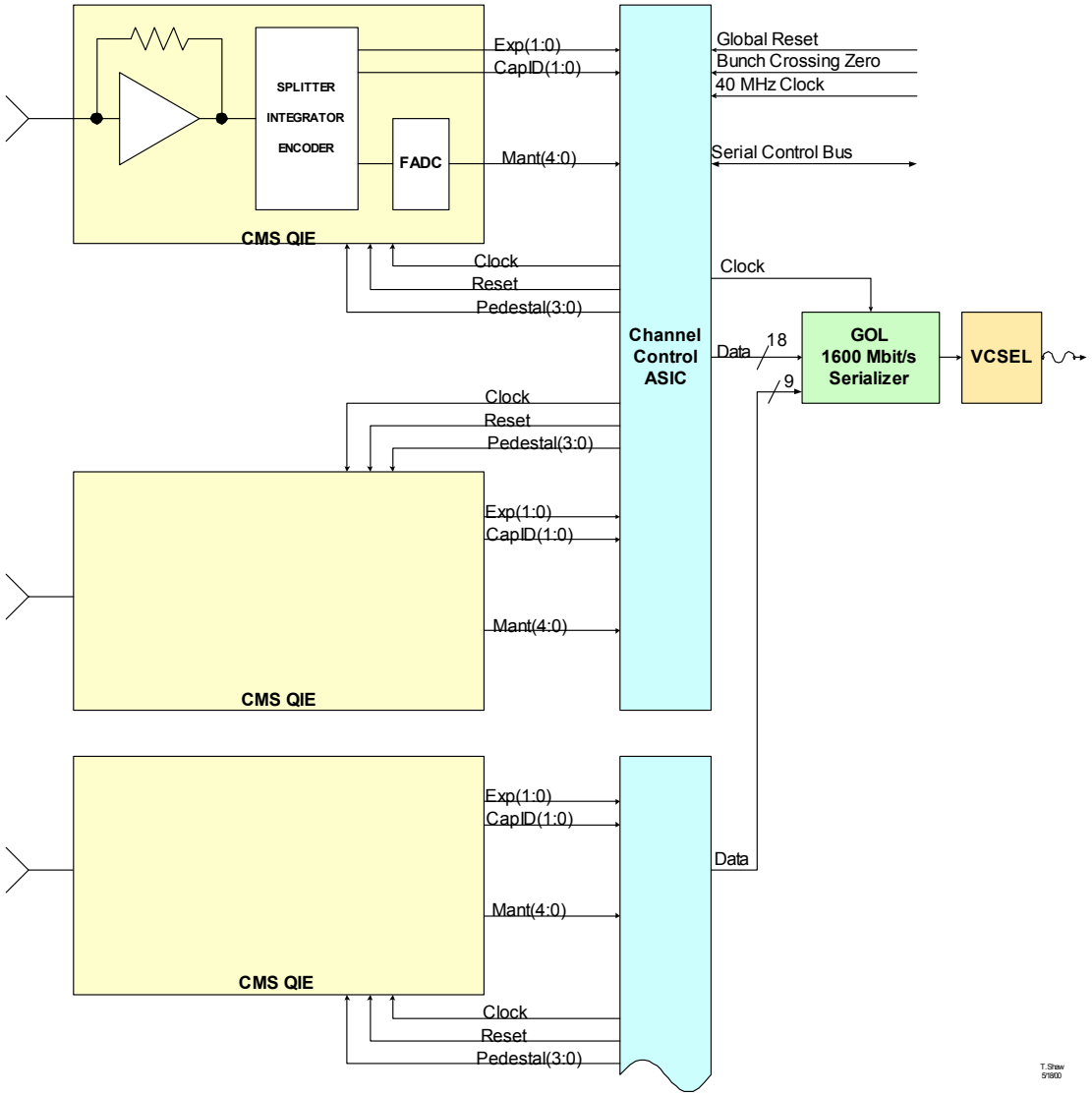
FE Status(1)

- **CCA**
  - Chips are being checked at automated teststand
- **QIE**
  - Testbeam parts did not run at 40MHz
  - Noise levels proved difficult to achieve
    - **3000-4000 e's rms with optimal layout**
  - 2 Production wafers back Oct 2002
  - QIEs work at 40MHz+
- **Proto GOL ASIC tested - ok**
  - Gigabit Ethernet protocol at 1.6 Gbits/s
  - 2 Engineering wafers out for Fab.
  - Design work under way for GOL tester

FE Status(2)

- Connectorized VCSEL tested – ok
- Voltage regulator tested - ok
- Radiation qualified the “glue” logic parts
- 144 channel Testbeam 2002 (33Mhz) – ok
- HB Backplanes are complete
- HE Backplane prototype exists

FE Channels


SPLITTER
INTEGRATOR
ENCODER
FADC
CMS QIE
Exp(1:0)
CapID(1:0)
Mant(4:0)
Clock
Reset
Pedestal(3:0)
Channel Control ASIC
Global Reset
Bunch Crossing Zero
40 MHz Clock
Serial Control Bus
Clock
Data
18
9
GOL 1600 Mbit/s Serializer
VCSEL
Data

QIE Description

QIE (already passed PRR)

Charge Integrator Encoder

4 stage pipelined device (25ns per stage)

- charge collection
- settling
- readout
- reset

Inverting (HPDs) and Non-inverting (PMTs) Inputs

Internal non-linear Flash ADC

Outputs

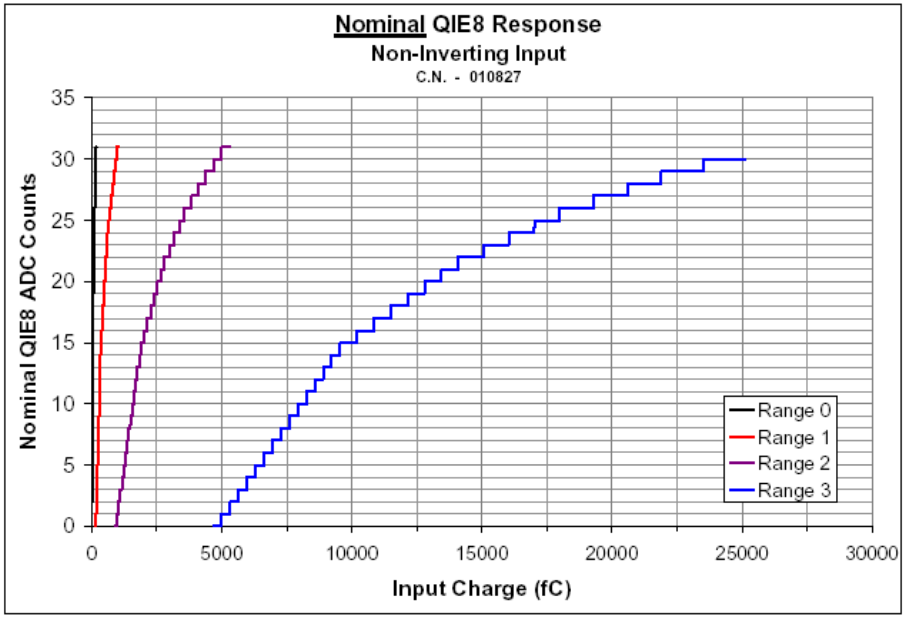
- 5 bit mantissa
- 2 bit range exponent
- 2 bit Cap ID

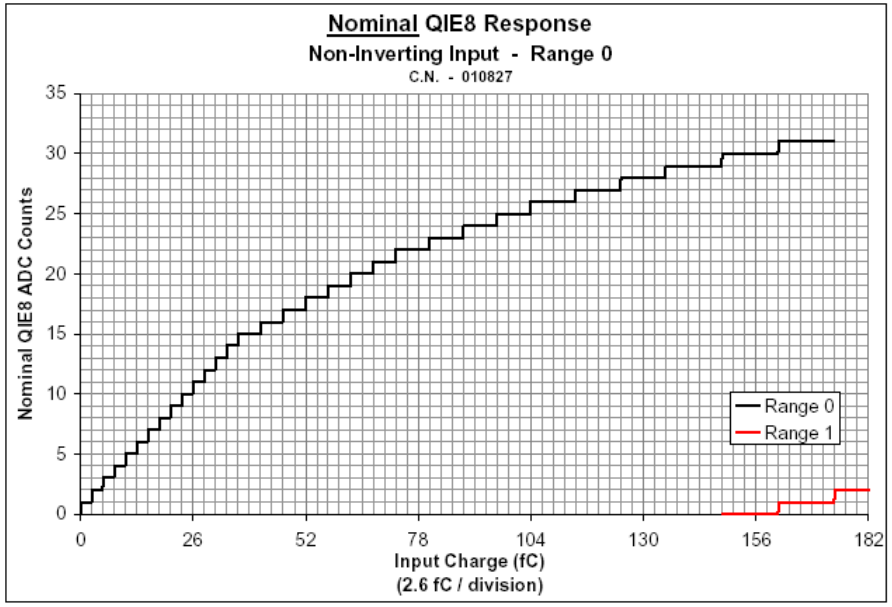
QIE Specification

QIE Design Specifications

- Clock > 40 MHz
- Must accept both polarities of charge
- Charge sensitivity of lowest range – 1fC/LSB(inverting-input)
  - In Calibration Mode 1/3 fC/LSB
- Maximum Charge – 9670 fC/25ns(inverting-input)
- 4500 electrons rms noise
- FADC Differential Non-Linearity < .05 LSBs

QIE Test Results



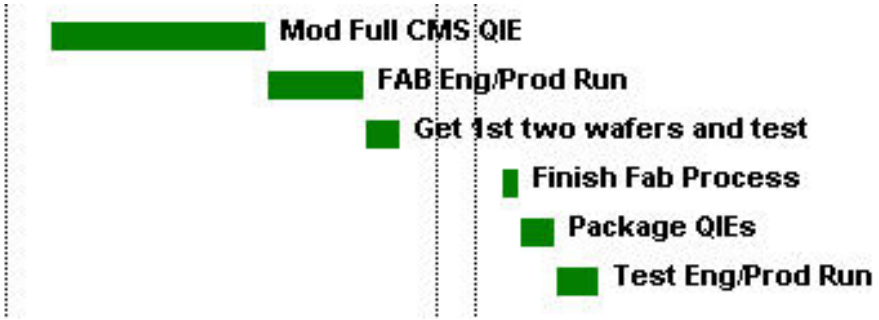


CMS QIE Production Schedule

Production QIE

- QIE modified to work at 40MHz
- 2 wafers arrived in early Oct ‘02
- Production hold on remainder of wafers
- ASIC tester verifies 40MHz operation
- Tested parts should be in hand Mar ‘03

Mod Full CMS QIE	Mon 2/4/02	120 days
FAB Eng/Prod Run w/Prod Halt	Mon 7/22/02	55 days
Get 2 wafers/Test/Package	Mon 10/7/02	20 days
Finish Production Wafers	Mon 1/20/03	10 days
Package QIEs	Mon 2/3/03	20 days
Test Eng/Prod Run	Mon 3/3/03	25 days



Channel Control ASIC

The CCA provides the following functions: **(Already passed PRR)**

- The processing and synchronization of data from two QIEs,
- The provision of phase-adjusted QIE clocking signals to run the QIE charge integrator and Flash ADC,
- Checking of the accuracy of the Capacitor IDs, the Cap IDs from different QIEs should be in synchronization,
- The ability to force the QIE to use a given range,
- The ability to set Pedestal DAC values,
- The ability to issue a test pulse trigger,
- The provision of event synchronization checks – a crossing counter will be implemented and checked for accuracy with every beam turn marker,
- The ability to send a known pattern to the serial optic link,
- The ability to “reset” the QIE at a known and determined time,
- And, the ability to send and report on any detected errors at a known and determined time.

CCA Status

Engineering/Production chip submitted March '02

- Wafers back
- Two wafers were packaged
- Used successfully in testbeam
- Remainder of wafers have been packaged
- CCA ASIC tester ready – chips being tested

Gigabit Optical Link (GOL) Configuration

- 32 bit mode; 1.6 Gb/s; Gigabit Ethernet Protocol
- Engineering order submitted and back from fab
- FNAL to help in production of ASIC tester
- Untested parts in hand Jan/Feb '03

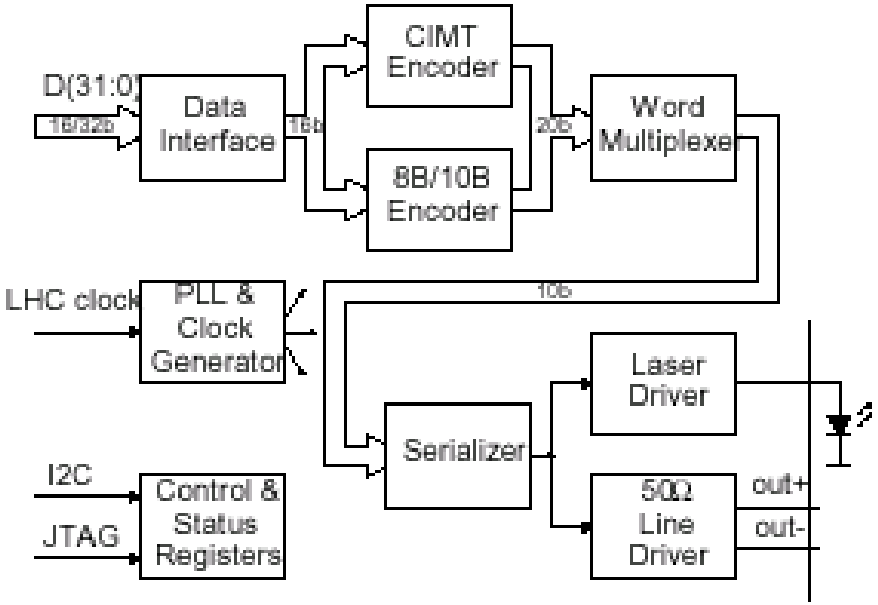
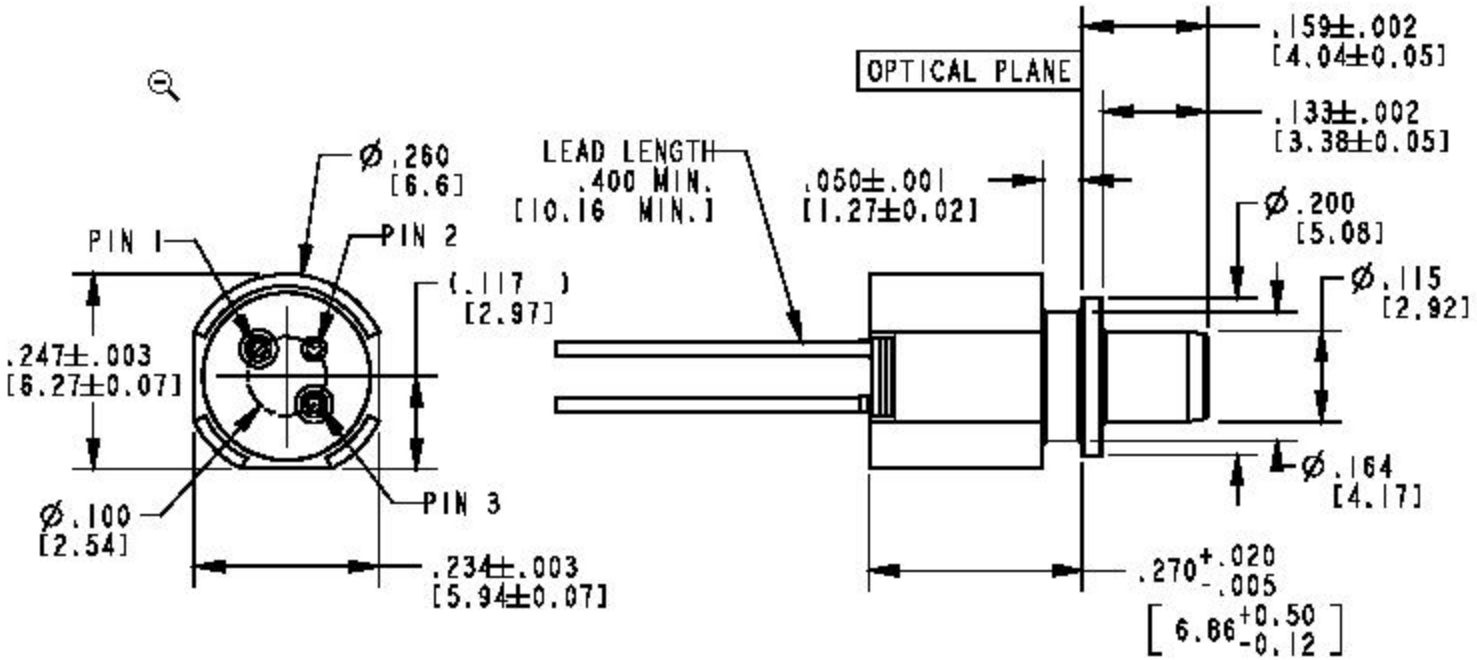


Figure 1 GOL block diagram.

Connectorized VCSEL (HPD Boards)

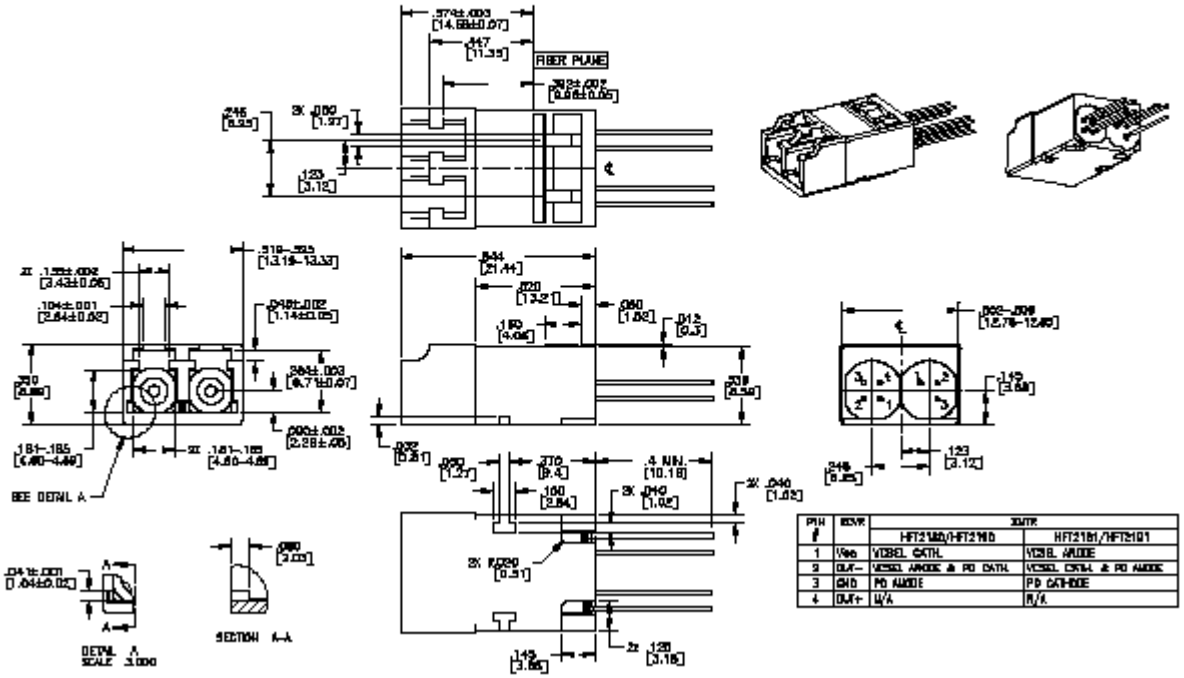
2.5Gbps VCSEL Connectorized - Datacom		
 NEW!	HFE419x-521  Product Sheet	LC Connectorized Components, Common Anode and Common Cathode, 2.5 Gb/s operation, attenuated



HF VCSEL (PMT Boards)

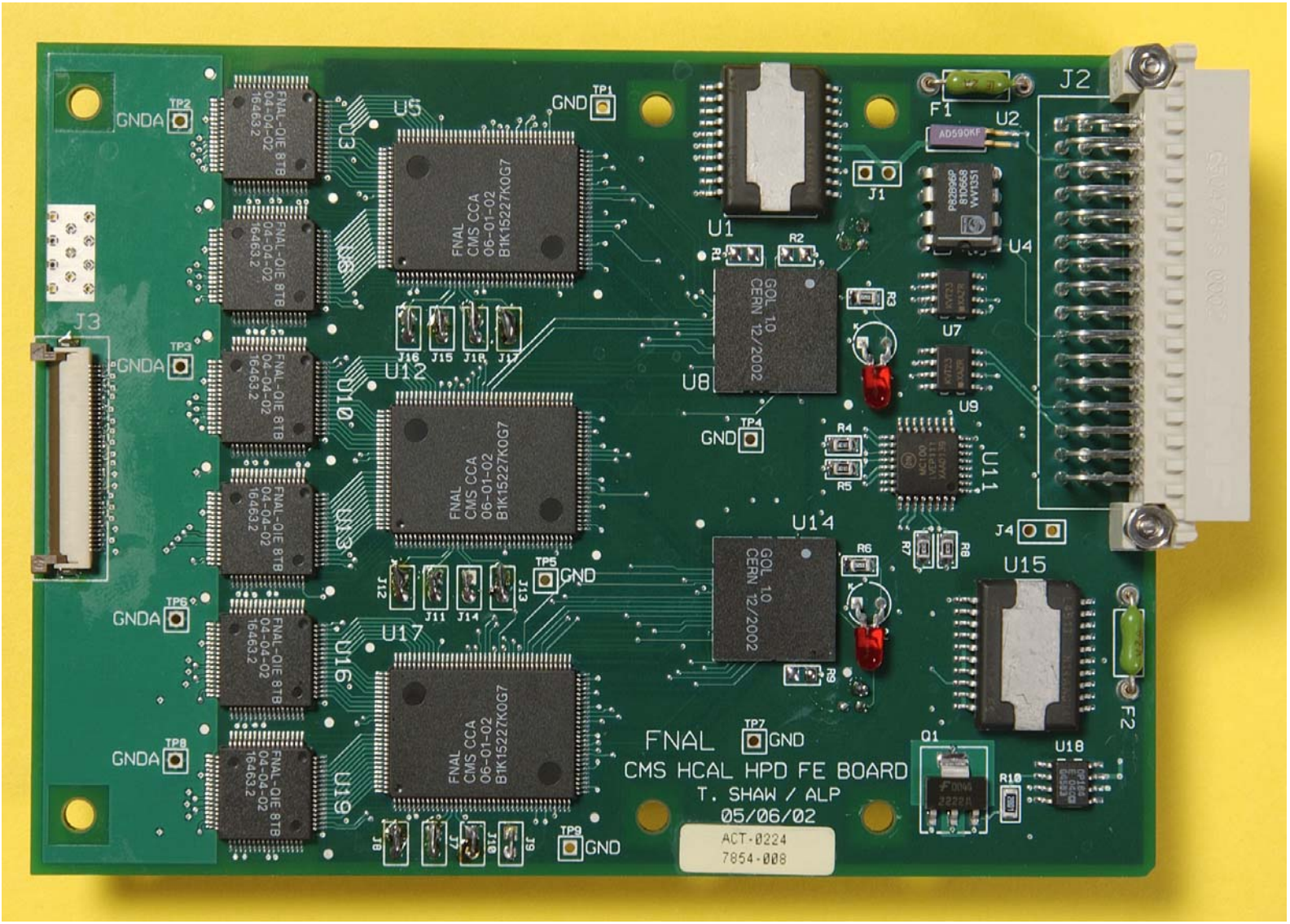
Fiber Optic LAN Components
LC SFF Duplex OFE 2.5 Gbps

HFT219x-541

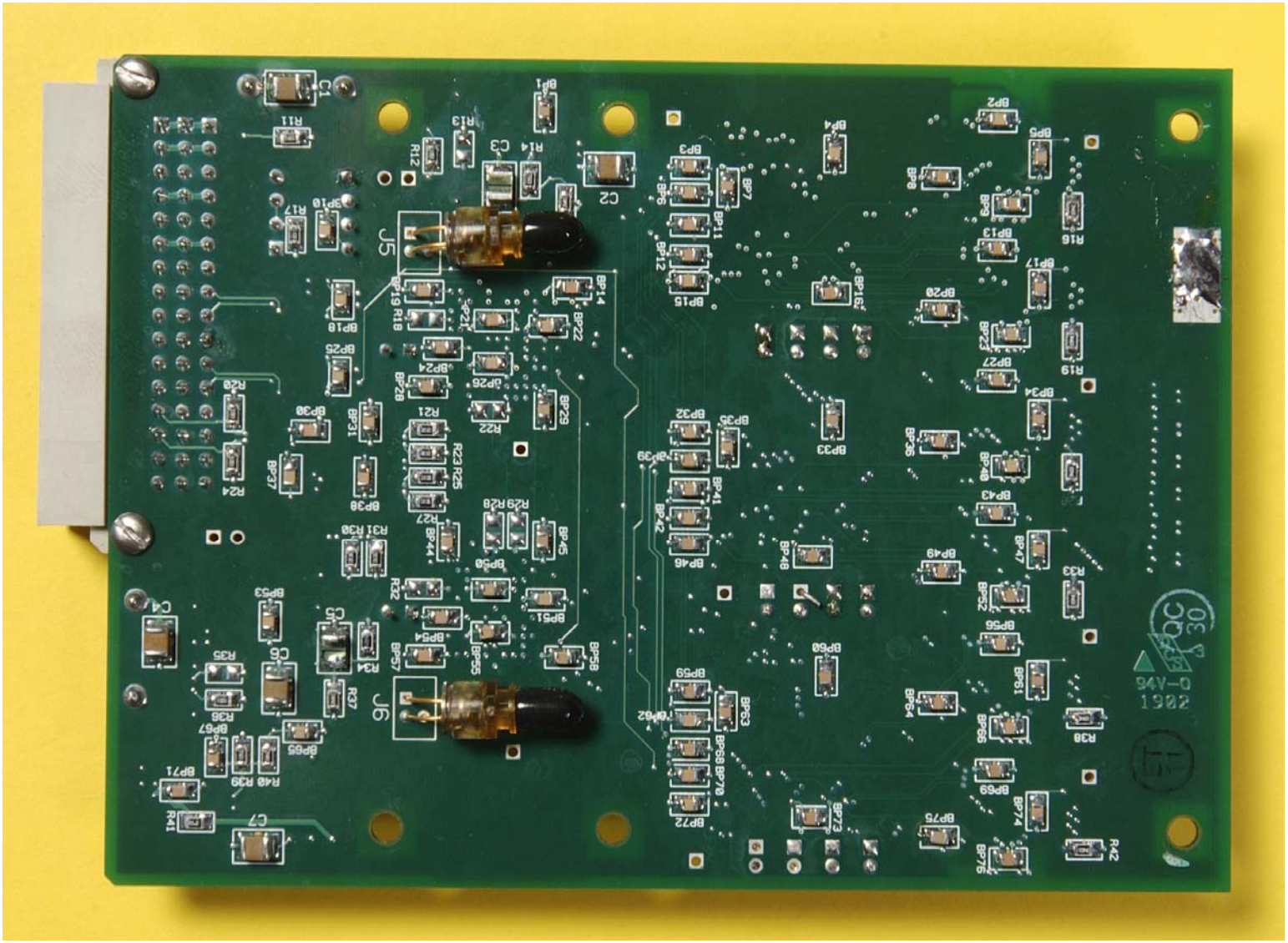


PIN #	ECVR	XCVR	
		HFT2181/HFT2191	HFT2181/HFT2101
1	VEE	VCSEL CATH.	VCSEL ANODE
2	OUT-	VCSEL ANODE & PD CATH.	VCSEL CATH. & PD ANODE
3	GND	PD ANODE	PD CATHODE
4	OUT+	N/A	N/A

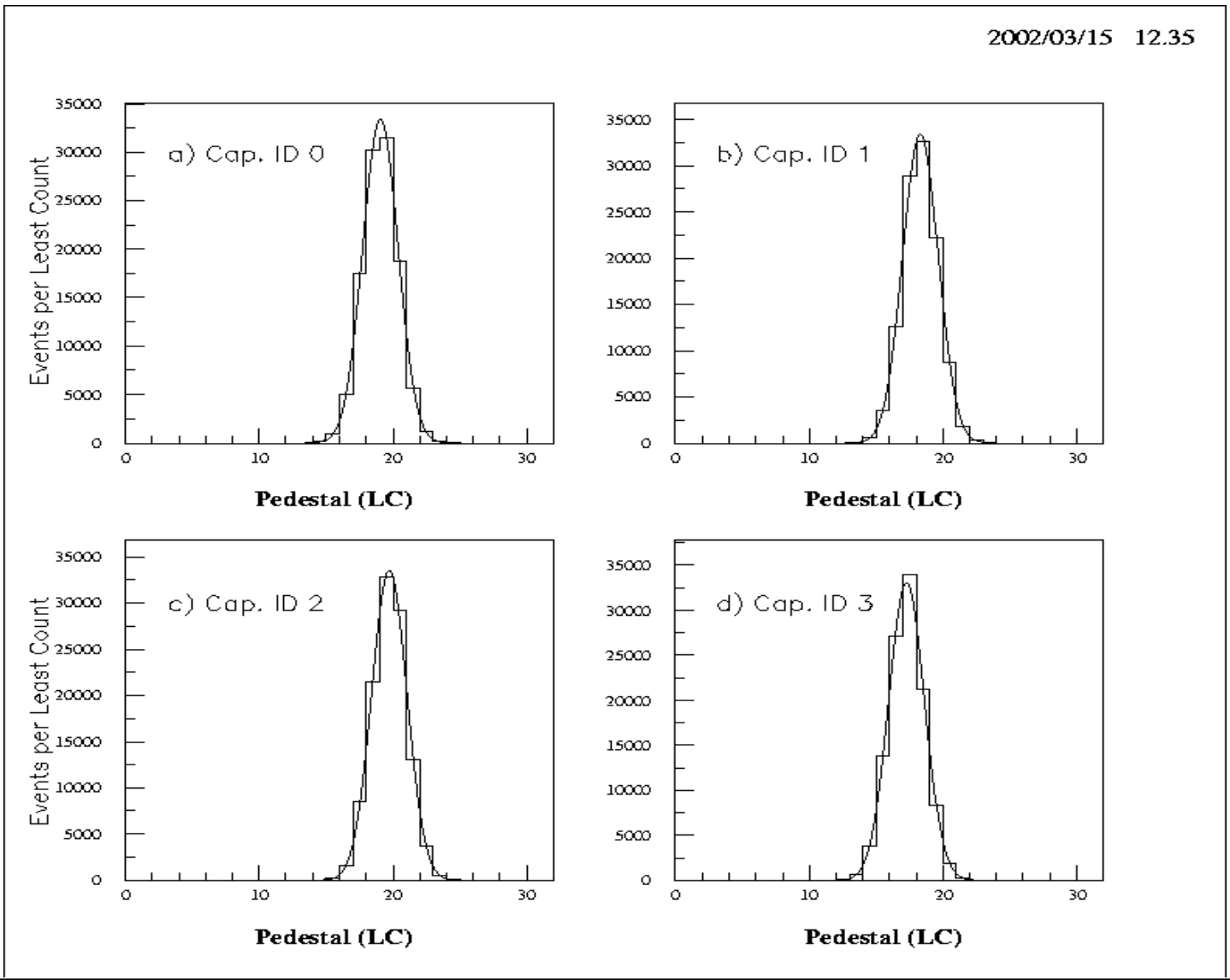
6 channel FE HPD Proto



6 channel FE HPD Proto

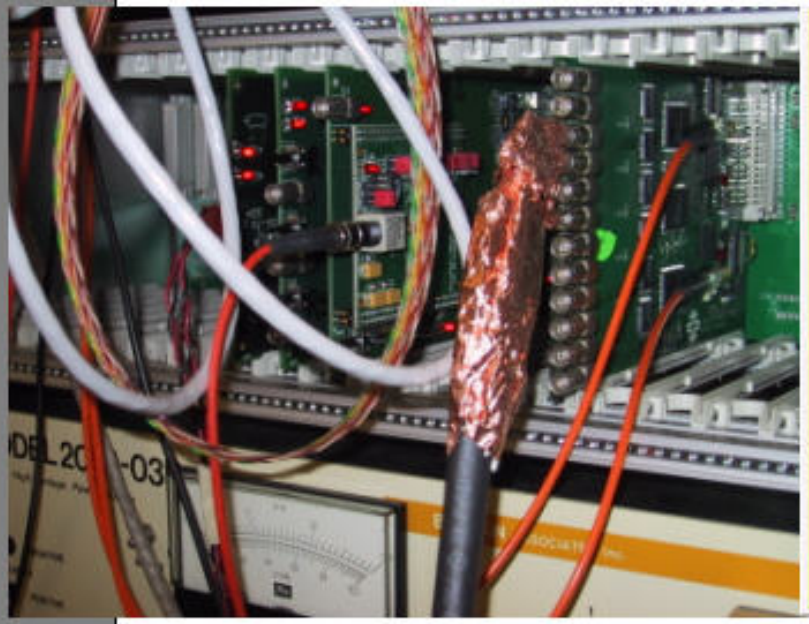


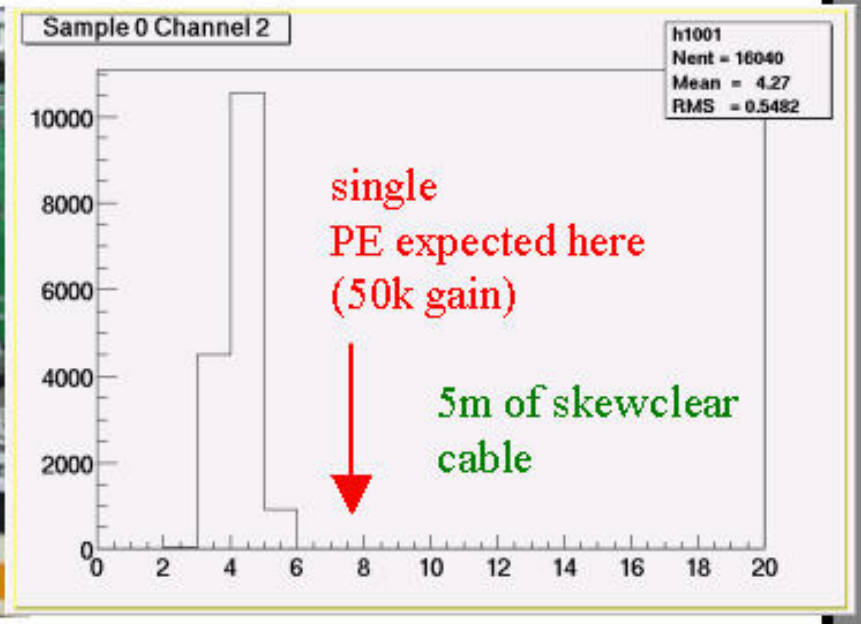
Pedestals 2800 e's rms



HF Electronics (PMT)

Forward Calorimeter Front-End (HF):





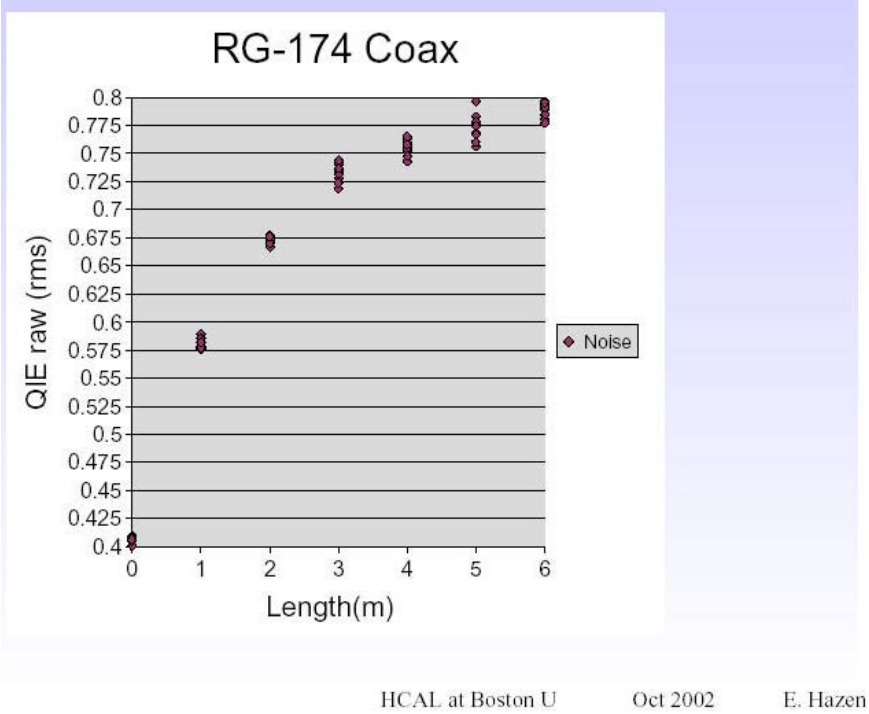
Boston University

Package of HCAL QIE in standard 3u VME crate with non-inverting input.

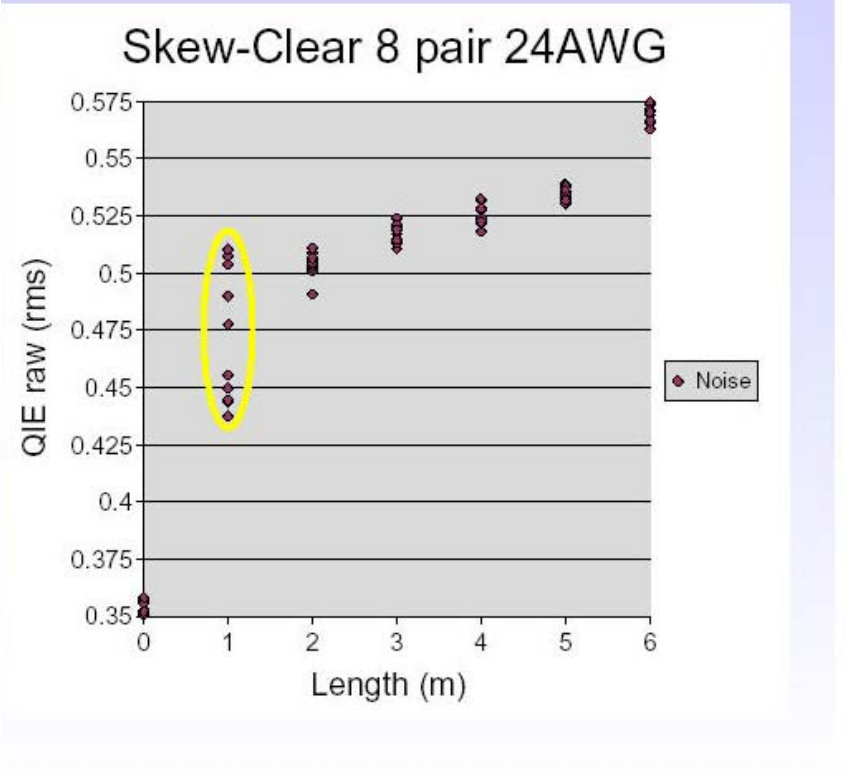
Connect QIE to phototubes (5m distant) without introducing excessive noise.

Will be used in CERN testbeam 2003 for HF calibration (18 wedges).

HF Cable tests



HCAL at Boston U Oct 2002 E. Hazen



HCAL at Boston U Oct 2002 E. Hazen

HF Status

HF Noise Test Summary

- PMT Test setup comissioned with QIE/HTR/DCC chain.
- Extensive testing done with two cable types, lengths from 1-6m:
  - Dual RG-174 coax with overall braid shield
  - Amphenol Skew-Clear(tm) 100 twisted pair
- Noise performance is excellent:
  - 9500e rms (1.5fC) for 6m skew-clear cable
  - 12500e rms (2.0fC) for 6m RG-174 coax cable

(single pe is 8fC for PMT gain of 5E4)

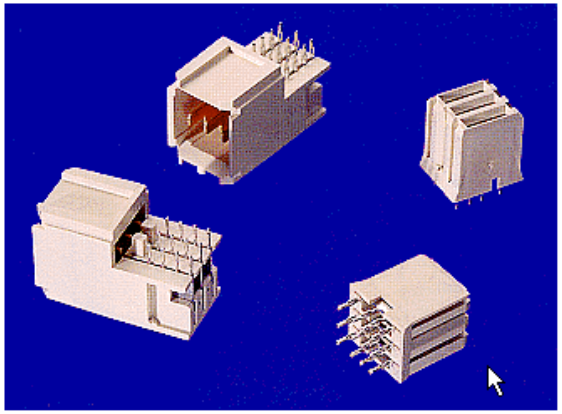
HCAL at Boston U Oct 2002 E. Hazen

Backplane Low Voltage Power Connector

Product Facts

- "Inverse-sex" design meets IEC 950 safety requirements
- Current rated at 7.8 amperes per contact, 23.5 amperes per module, fully energized
- Sequenced right-angle headers available for "make-first/break-last" applications
- ACTION PIN press-fit contacts on both headers and receptacle
- Contacts designed for up to 250 mating cycles
- Recognized to U.S. and Canadian requirements under the Component Recognition Program of Underwriters Laboratories Inc.

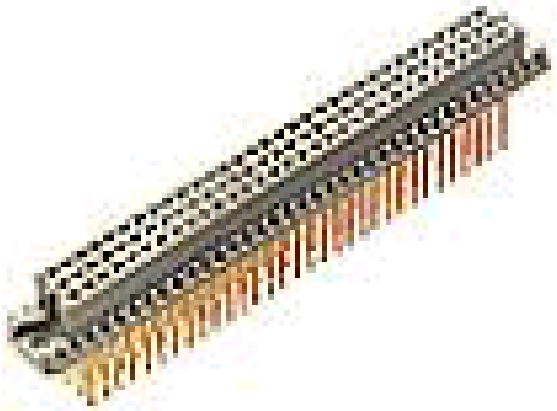
Universal Power Module

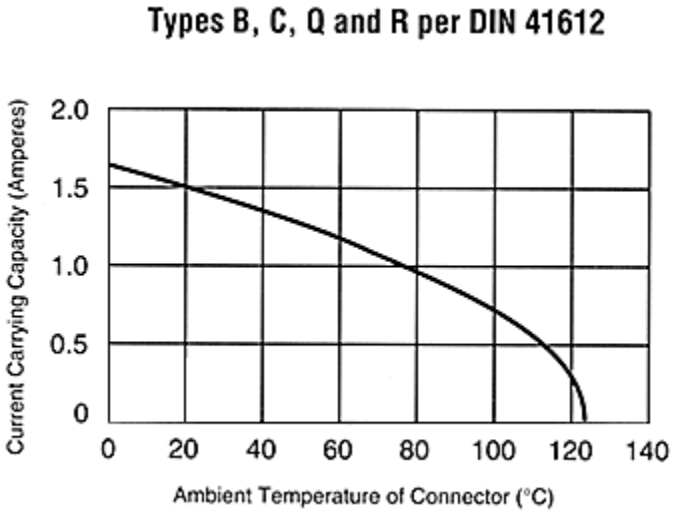


Backplane Connectors

Type C and Enhanced Type C Assemblies

Minimum adjacent mounting space required:
12.7 [.500]
Current Rating:
Per DIN 41612*
Voltage Rating:
250 VAC
Dielectric Rating:
1000 VAC
Contact Resistance:
15 milliohms initial at 100 ma and 50 mv, open circuit





HCAL RBX Backplane Signals

Pin Number	Row A	Row B	Row C
1	GND	GND	GND
2	V1	V1	V1
3	GND	GND	GND
4	V2	V2	V2
5	GND	GND	GND
6	V2	V2	V2
7	GND	GND	GND
8	MCLK+	GND	SERCLK+
9	MCLK-	GND	SERCLK-
10		GND	SER_DAT
11	TEMP	GND	RESET_PLL+
12		GND	RESET_PLL-
13	GEO_ADDR(0)	GND	RESET+
14	GEO_ADDR(1)	GND	RESET-
15	BZERO+	GND	PWR_RESET
16	BZERO-	GND	PWR_Trip

Table 2. FE Module Backplane Signals

V1 (power)

- Input voltage of 6.5V, which is regulated on board to 5.0V. This supplies power to the QIEs and temperature transducer.

V2 (power)

- Input voltage of 4.5V, which is regulated on board to 3.3V and 2.5V. This supplies power to all parts other than QIEs and the temperature transducer.

HCAL RBX Backplane Signals

MCLK+/- (input)

- Differential LVPECL signal which supplies the 40MHz LHC clock signal.

TEMP (output)

- Single ended line which provides a temperature measurement from the module. This is the output of a temperature transducer.

GEO_ADDR(1:0) (input)

- Geographic address pin on the backplane. The two pins provide address encoding for slot position within a group of three modules, see Table 3. These pins have weak pull-ups on the FE modules, so that grounded pins have an address of logic “0”, and floating pins have a logic level of “1”.

BZERO+/- (input, active high)

- Differential LVPECL signal which supplies the “Beam_Zero” marker. The “Beam_Zero” signal is required to reset the QIEs. The CCA is actually tasked with issuing a QIE_Reset, but does not do so until it senses a Beam_Zero.At least one Beam_Zero signal must be sent across the backplane before the FE module will be in a working state.

- The Beam_zero signal also triggers the CCA to output an “Orbit Message” to the GOL in place of normal QIE data.

HCAL RBX Backplane Signals

RESET+/- (input, active low)

- Differential LVPECL signal which supplies the reset signal to the CCA. This reset signal must be sent at or after power up in order to ensure the proper operation of the CCA. In addition, this reset will reset all CCA register values to the default value.

RESET_PLL+/- (input, active low)

- Differential LVPECL signal which supplies the reset signal to the GOL and the CCA's Delay Lock Loop. This reset signal must be sent at or after power up in order to ensure the proper operation of the GOL and CCA. In addition, this reset will reset the CCA delay lock loop, without effecting the CCA register values.

PWR_RESET (input, active high)

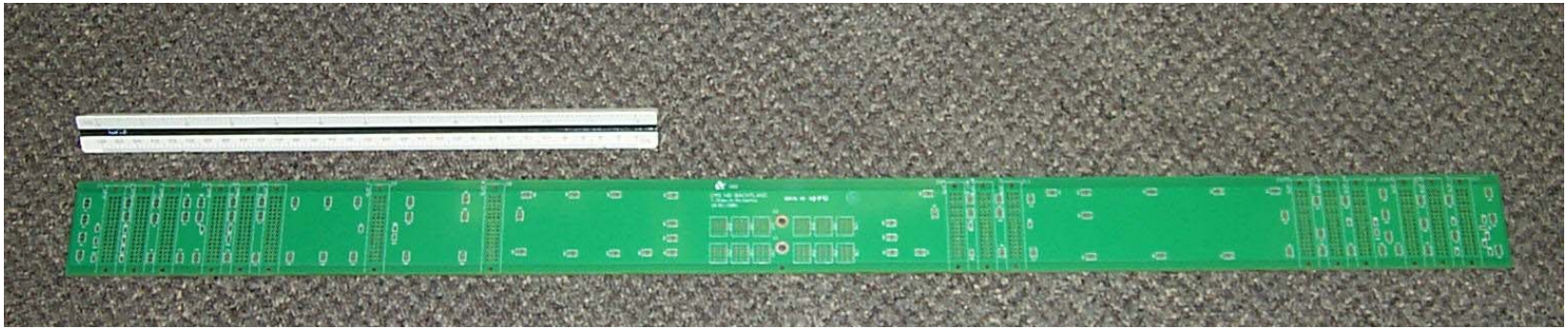
- Single-ended LVTTL signal used to reset the power circuit of the FE Module. This must be applied after power is initially applied to the circuit, prior to any other operations, as well as whenever an over current trip of the power circuit has occurred.

PWR_Trip (output, active high)

- A wired-or line which will signal that a FE module has had an over current trip.

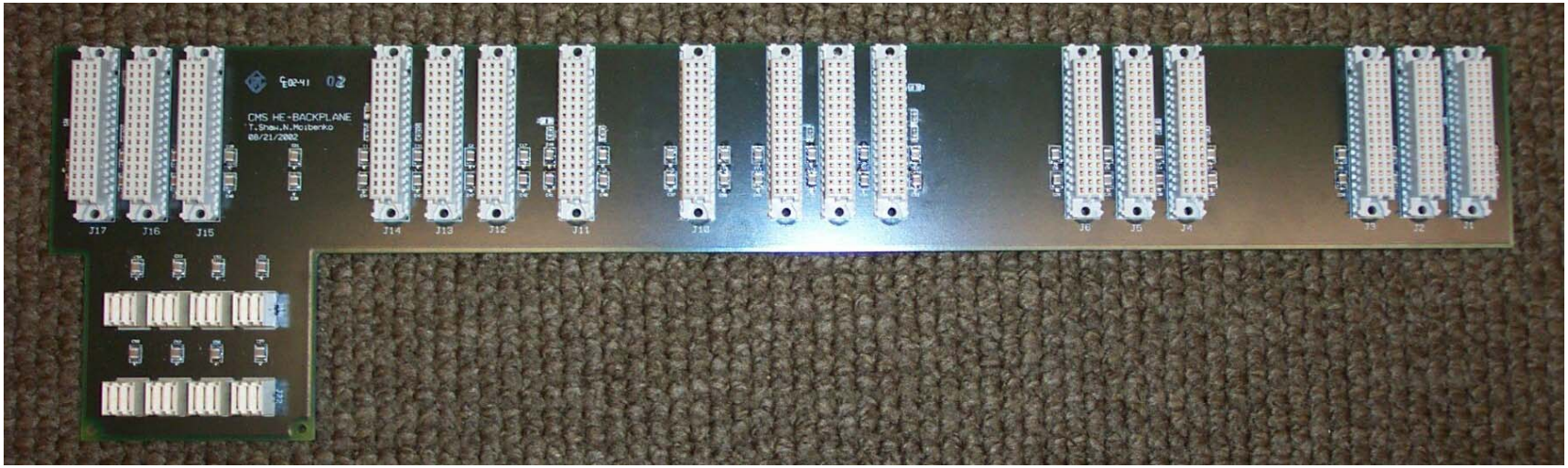
HB Backplanes

~87 CM LONG

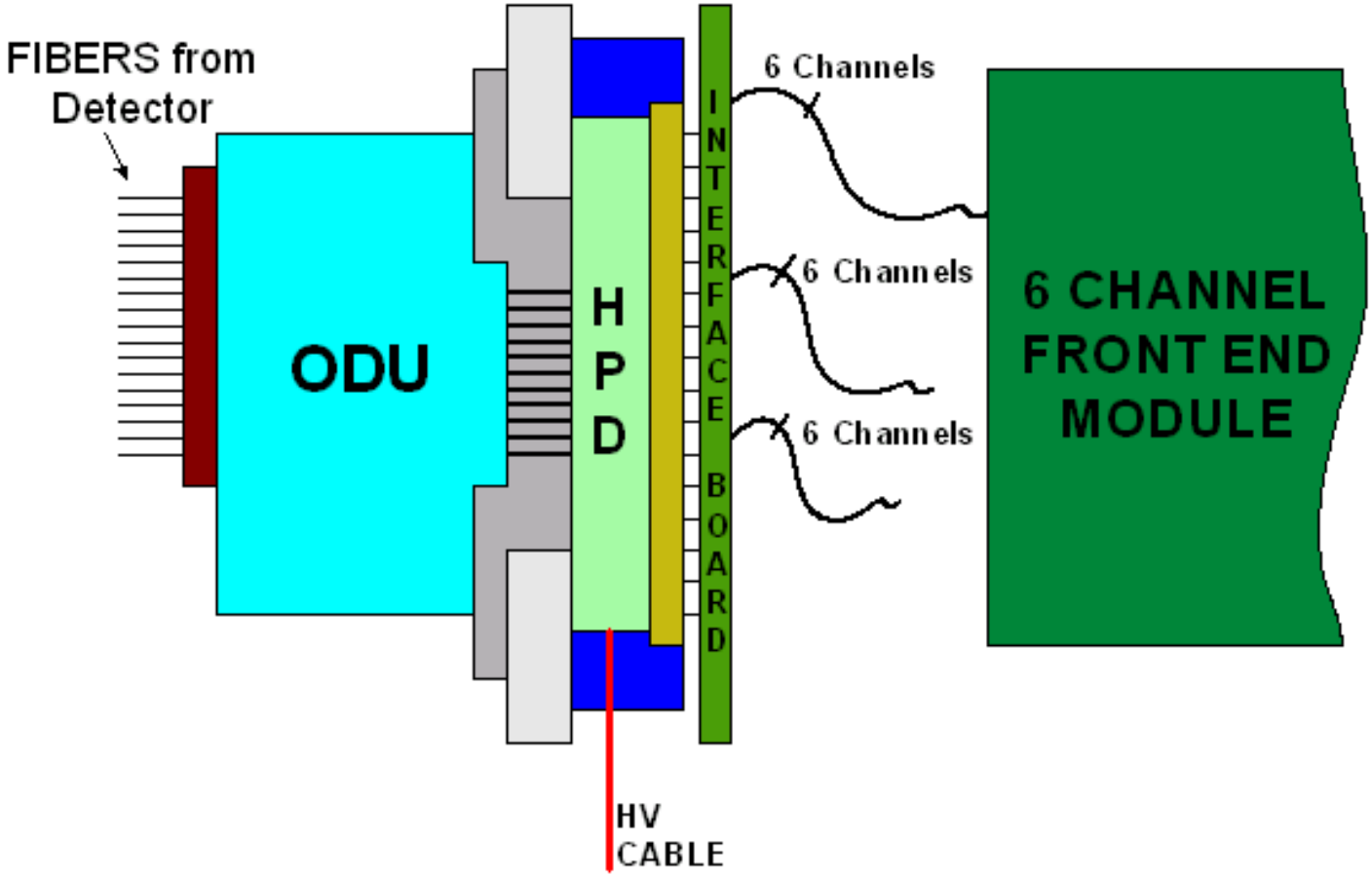


HE Backplane

Prototype



Readout Module Overview

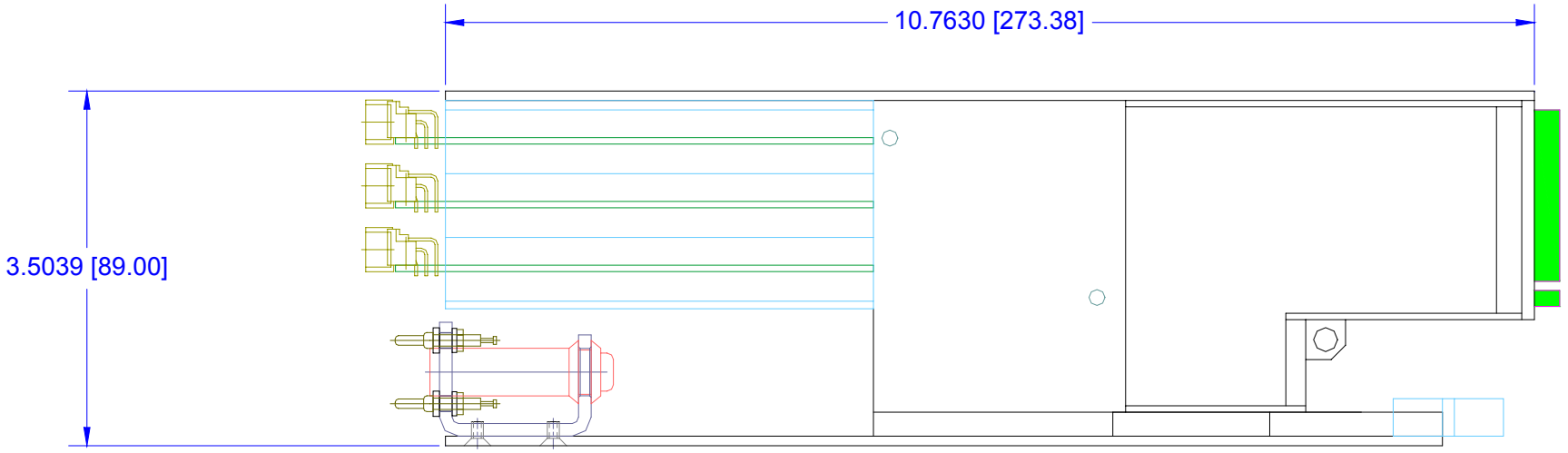


FFC Signal Cable

0.5 mm pitch

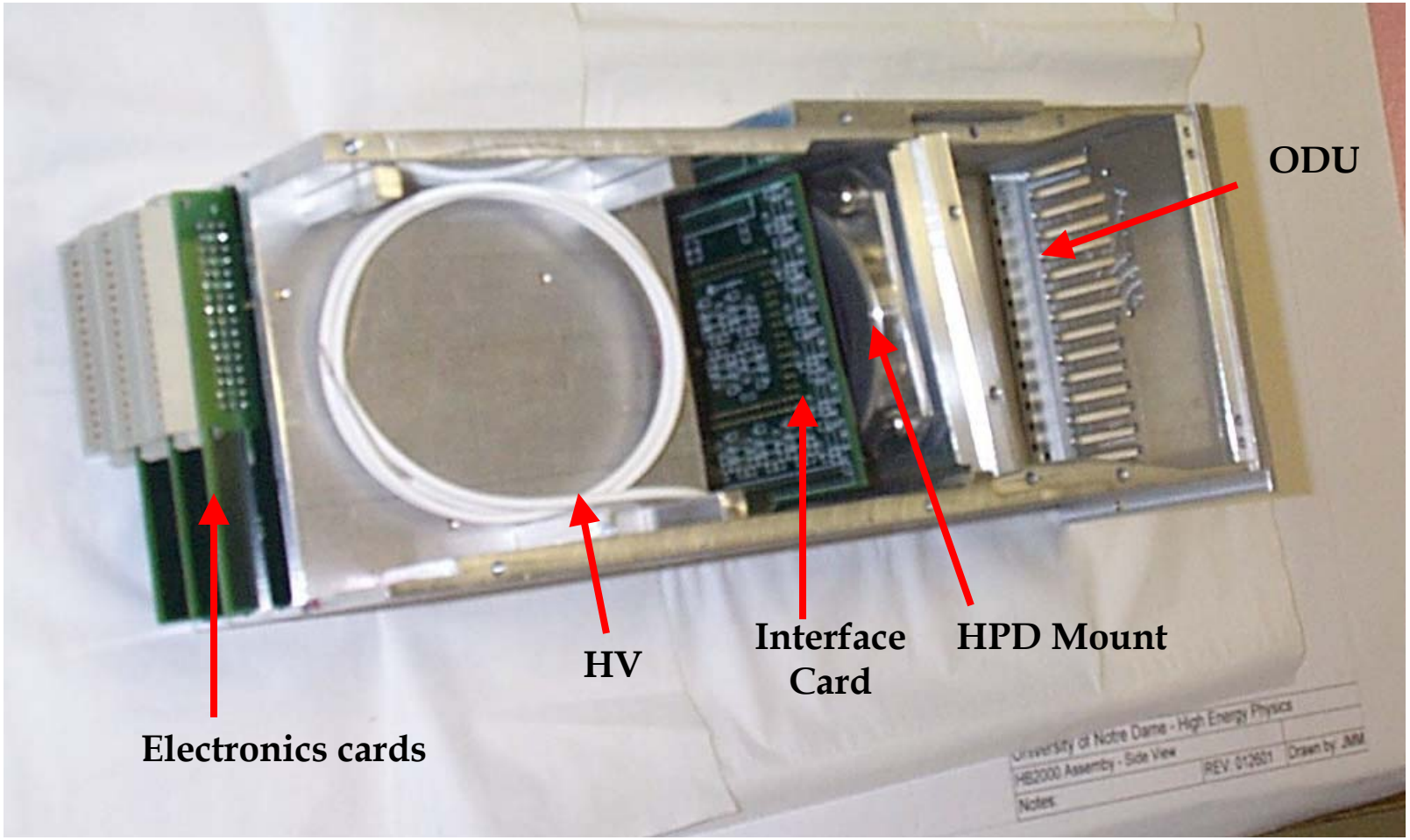
Flat Flex Cable

RM-19 Plan View

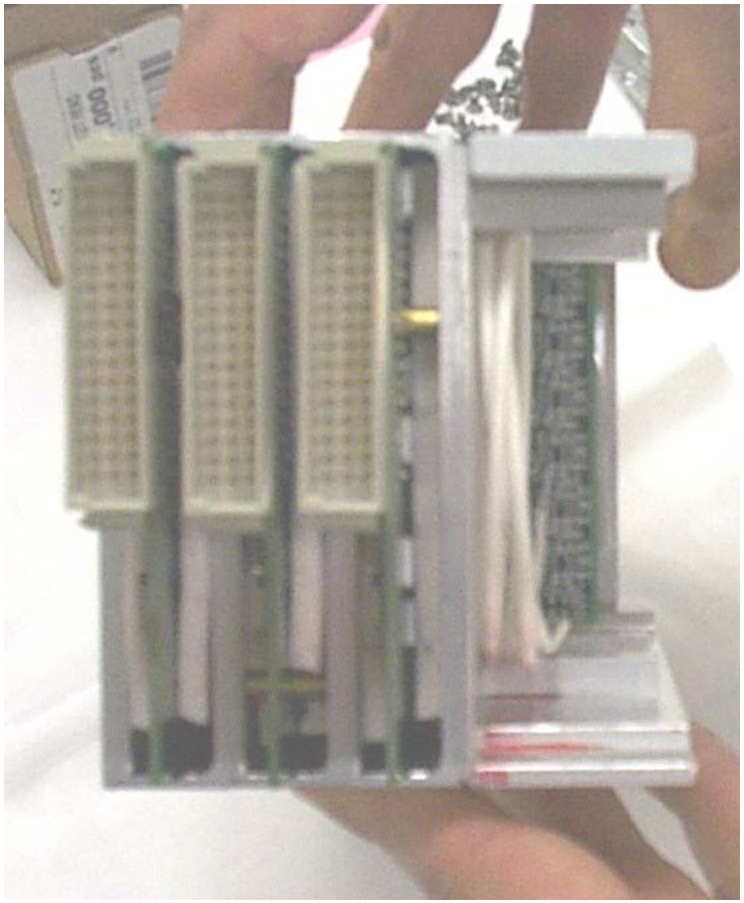


RBX Readout Module

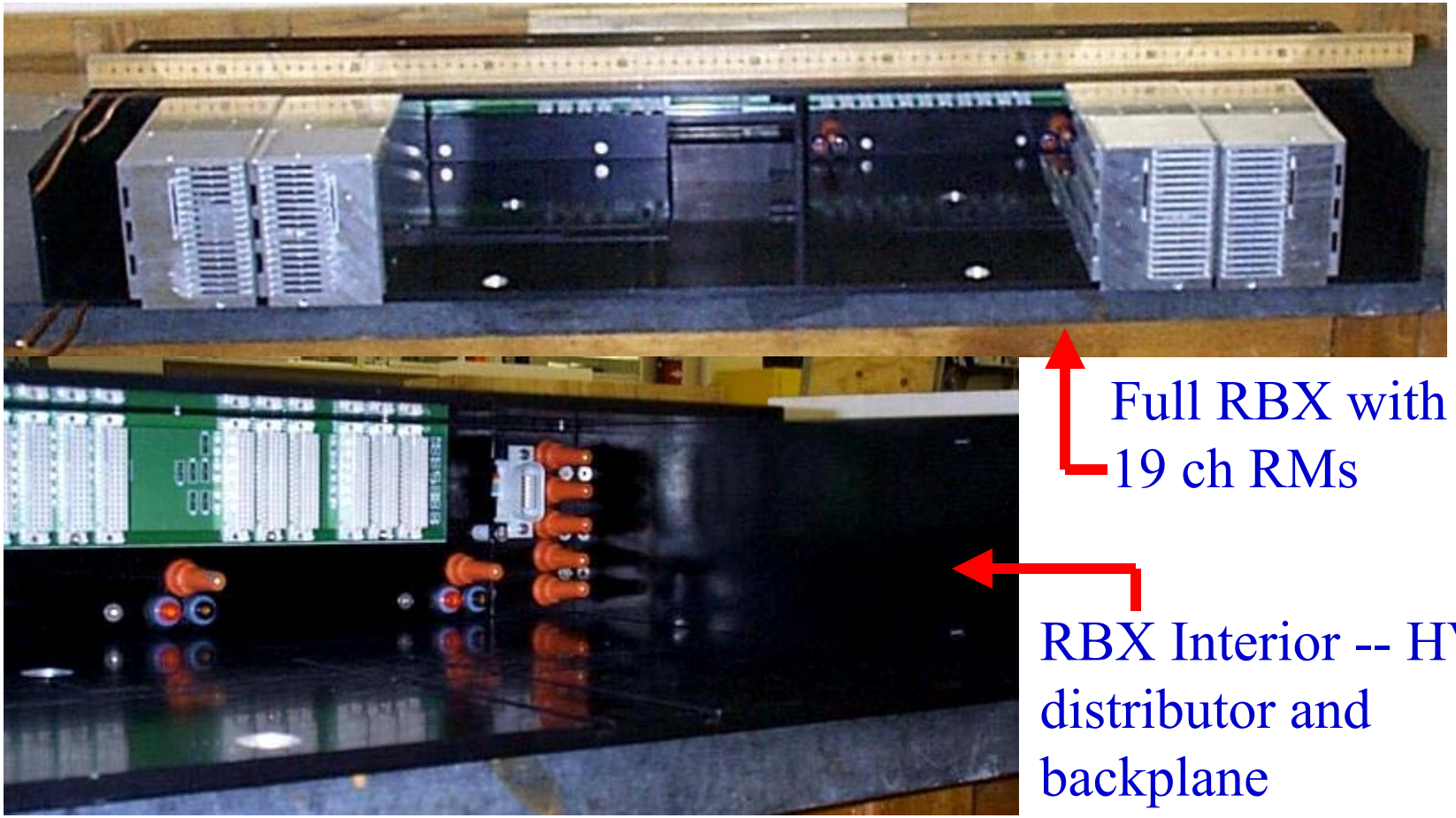
- The readout module (RM) integrates the HPD, front end electronics, and digital optical drivers.



RM19 Rear and Front Views



HB RBX Assembly



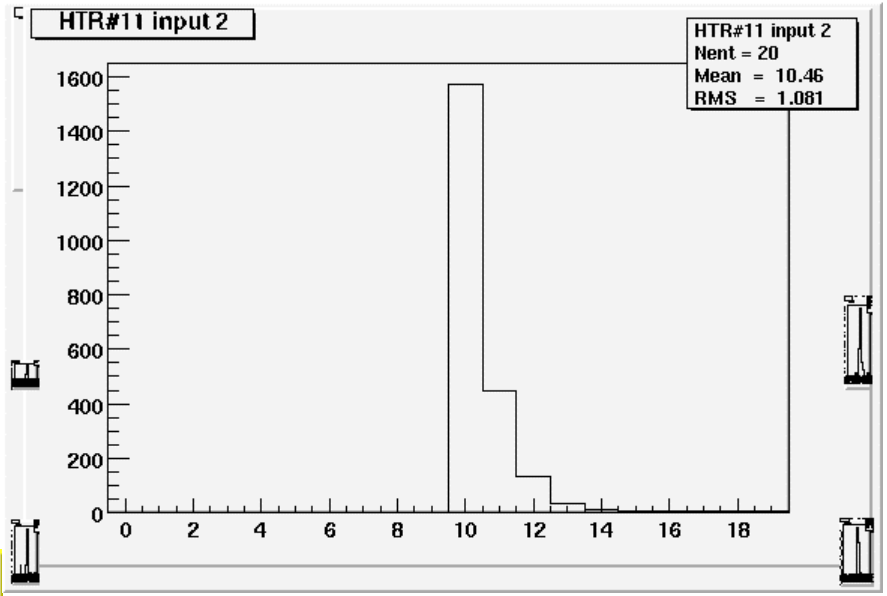
Full RBX with 19 ch RMs

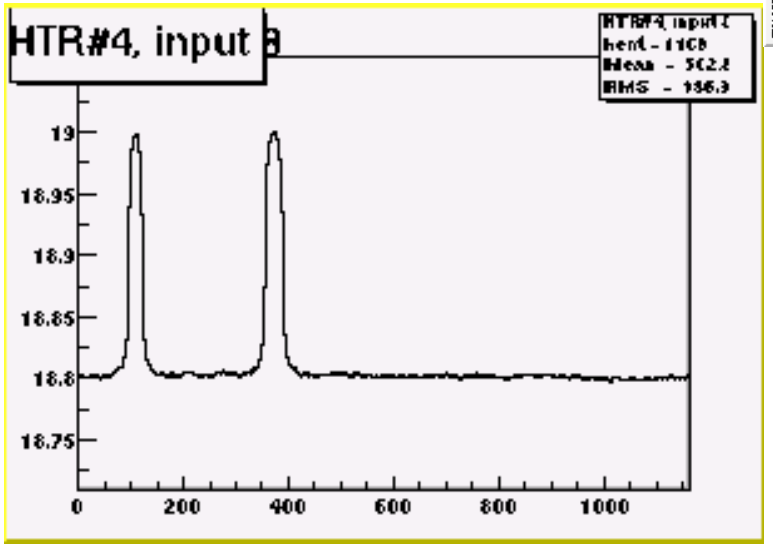
RBX Interior -- HV distributor and backplane

Testbeam 2002

Testbeam Plots

300 GeV pions





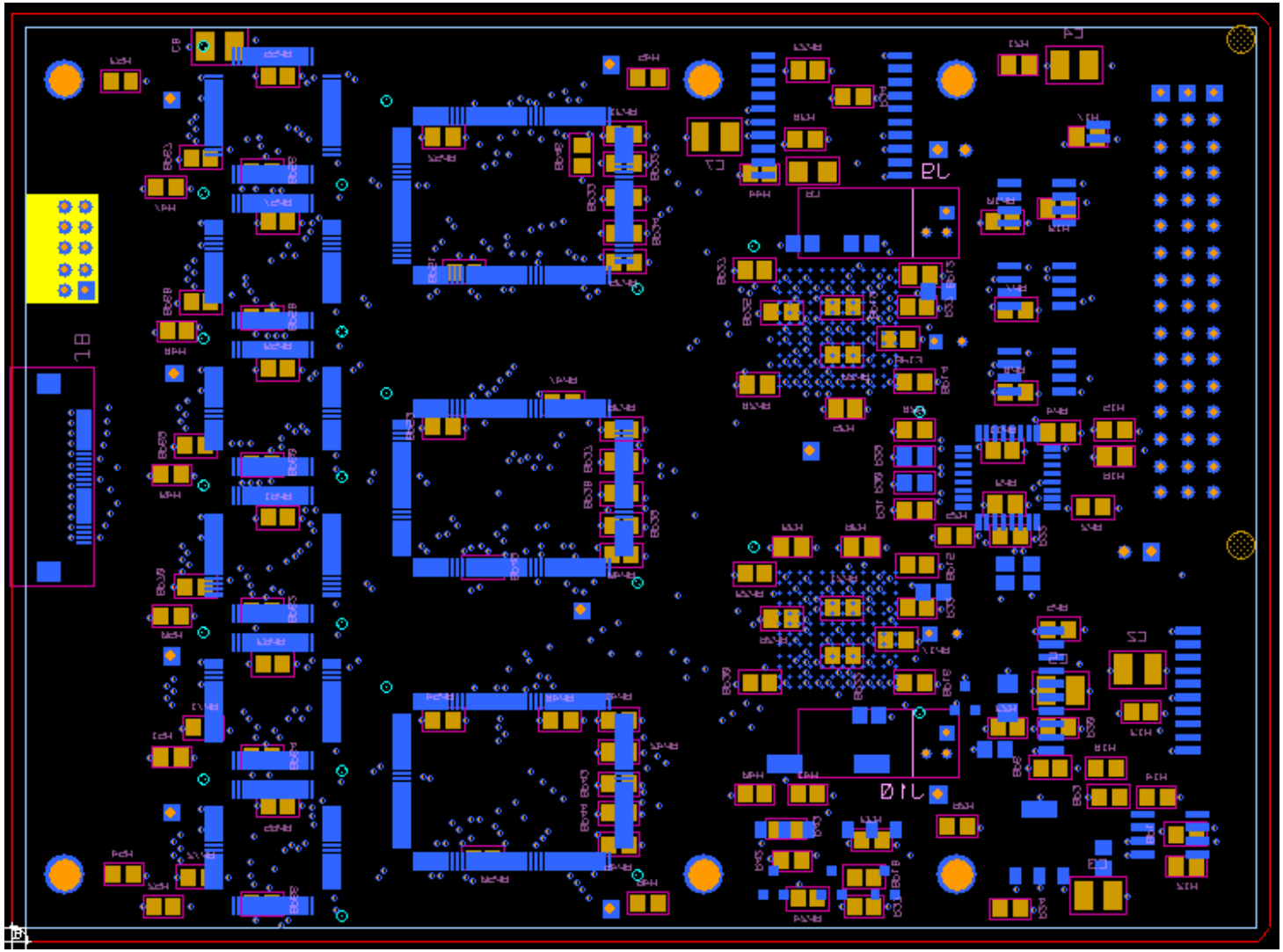
Sourcing

Pre-Production 6 Channel Module

Modifications from TB2002 Module

- New QIE pinout
- No fusing
- New Power trip circuitry with reset
- Improved Flat Flex Cable (FFC) connector
- New Grounding cable(s)

Pre-Production 6 Channel Module



ASIC yields/spares

QIE

- We are assuming a 70% yield, and buying 40% spares

CCA

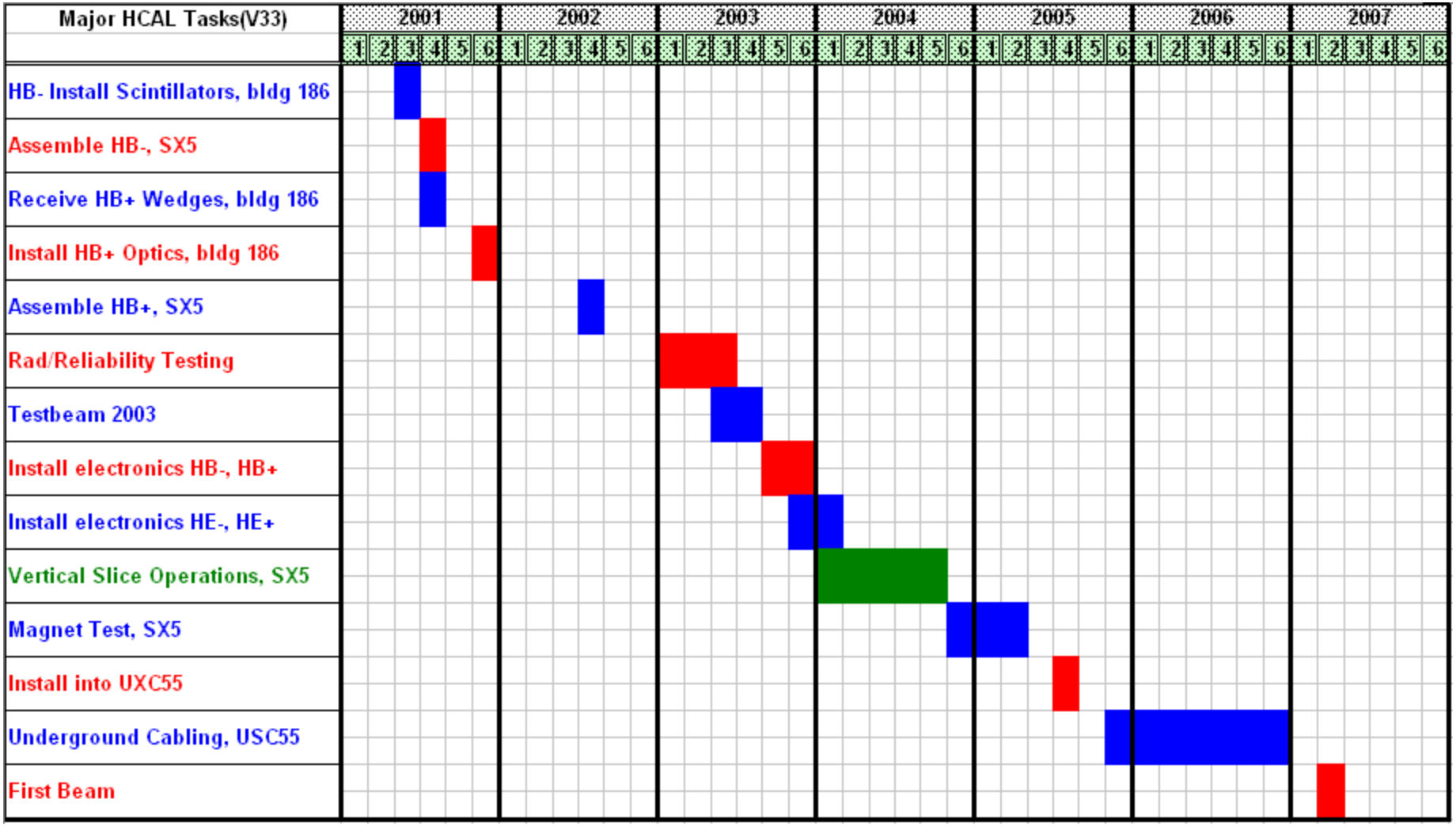
- We are assuming a 70% yield, and buying 40% spares

All other chips are bought tested.

20% spare cards for FE electronics

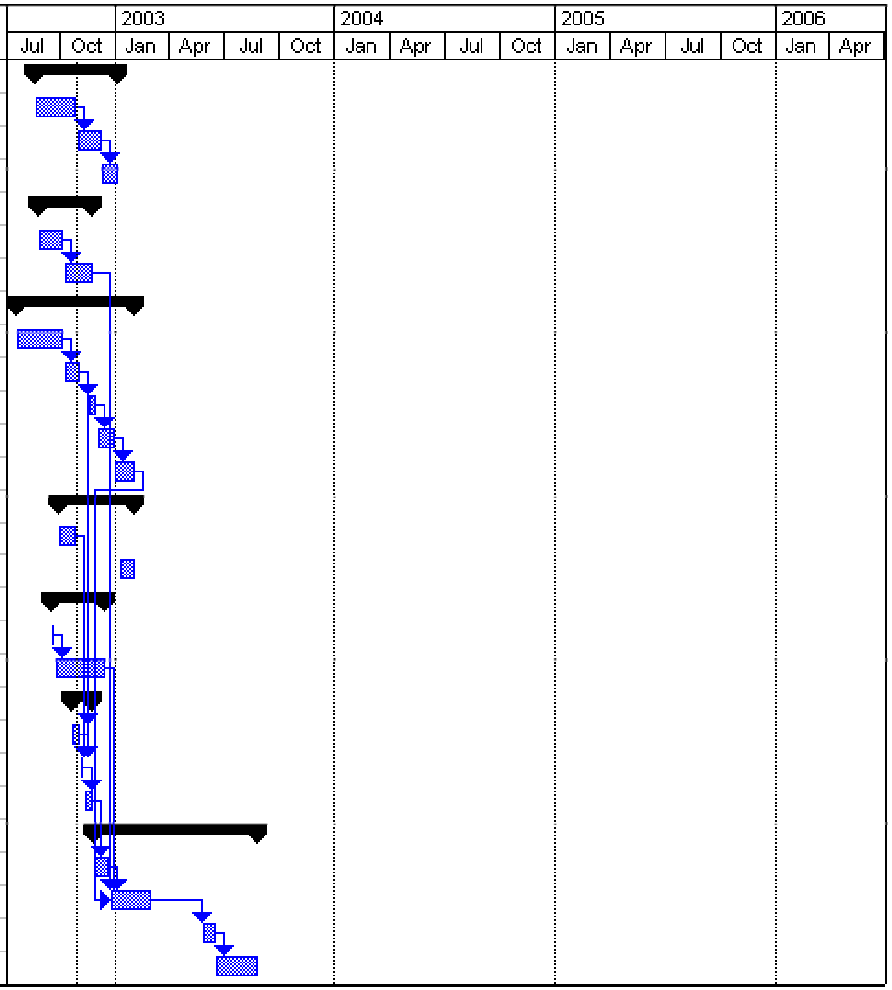
40% spare ASICs will be purchased

Front End Timeline



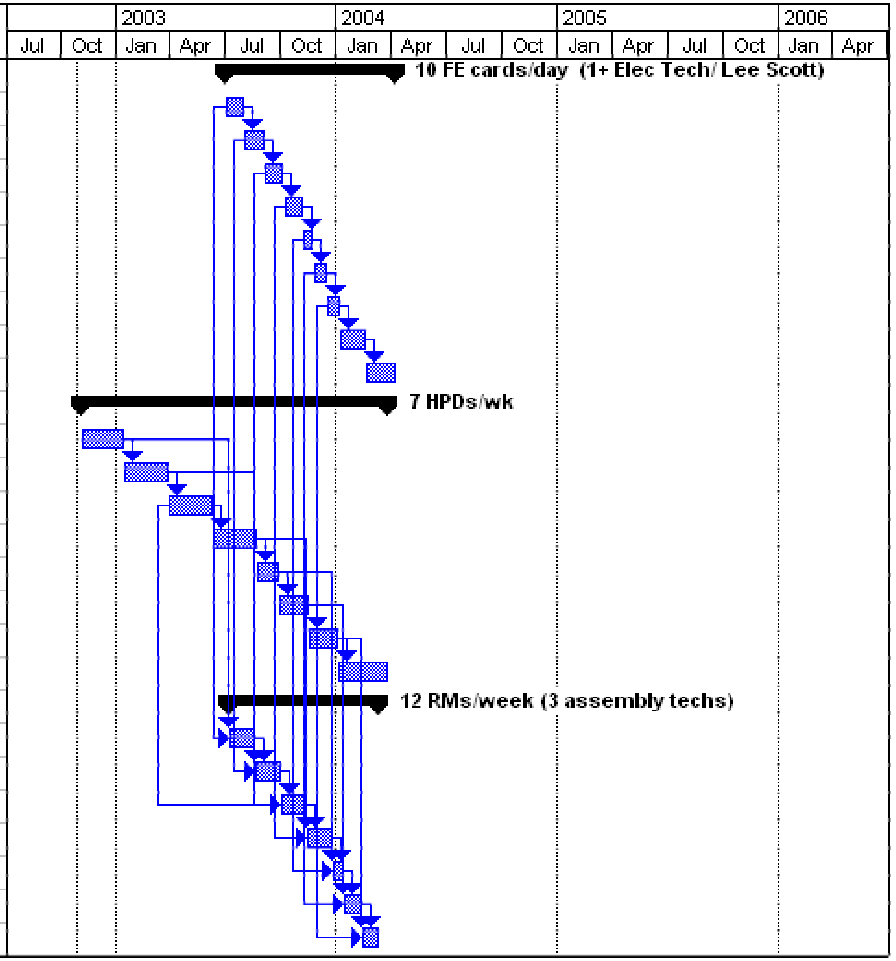
FE Production Schedule

ID	Task Name	Duration	Start	Finish
1	**GOL Production**	**100 days**	**Mon 8/19/02**	**Fri 1/3/03**
2	Fabricate	50 days	Mon 8/19/02	Fri 10/25/02
3	Package	30 days	Mon 10/28/02	Fri 12/6/02
4	Test	20 days	Mon 12/9/02	Fri 1/3/03
5	**CCA Production**	**65 days**	**Mon 8/26/02**	**Fri 11/22/02**
6	Package parts	30 days	Mon 8/26/02	Fri 10/4/02
7	Test Parts	35 days	Mon 10/7/02	Fri 11/22/02
8	**QIE Production**	**140 days**	**Mon 7/22/02**	**Fri 1/31/03**
9	Fabricate	55 days	Mon 7/22/02	Fri 10/4/02
10	Get/package 1st two wafers	20 days	Mon 10/7/02	Fri 11/1/02
11	Finish Fab of 24 wafers	10 days	Mon 11/18/02	Fri 11/29/02
12	Package 24 wafers	20 days	Mon 12/2/02	Fri 12/27/02
13	Test QIEs (2 techs)	25 days	Mon 12/30/02	Fri 1/31/03
14	**RD49 LV Regulators**	**90 days**	**Mon 9/30/02**	**Fri 1/31/03**
15	1000 parts avail. Sept '02	20 days	Mon 9/30/02	Fri 10/25/02
16	50000 parts avai early '03	20 days	Mon 1/6/03	Fri 1/31/03
17	**Commercial Parts**	**65 days**	**Mon 9/16/02**	**Fri 12/13/02**
18	Order Parts	5 days	Mon 9/16/02	Fri 9/20/02
19	Receive Parts	60 days	Mon 9/23/02	Fri 12/13/02
20	**Pre-Prod PCBs (new QIE/power/gnd/cable)**	**25 days**	**Mon 10/21/02**	**Fri 11/22/02**
21	Order Boards	10 days	Mon 10/21/02	Fri 11/1/02
22	Assemble	5 days	Mon 11/4/02	Fri 11/8/02
23	Test	10 days	Mon 11/11/02	Fri 11/22/02
24	**Produce/Assemble FE modules**	**195 days**	**Mon 11/25/02**	**Fri 8/22/03**
25	Order200+ Boards (TB/Rad/Reliability)	20 days	Mon 11/25/02	Fri 12/20/02
26	Assemble Boards (TB/Rad/Reliability)	50 days	Mon 12/23/02	Fri 2/28/03
27	Order Boards - Production	15 days	Mon 5/26/03	Fri 6/13/03
28	Assemble Boards - Production	50 days	Mon 6/16/03	Fri 8/22/03



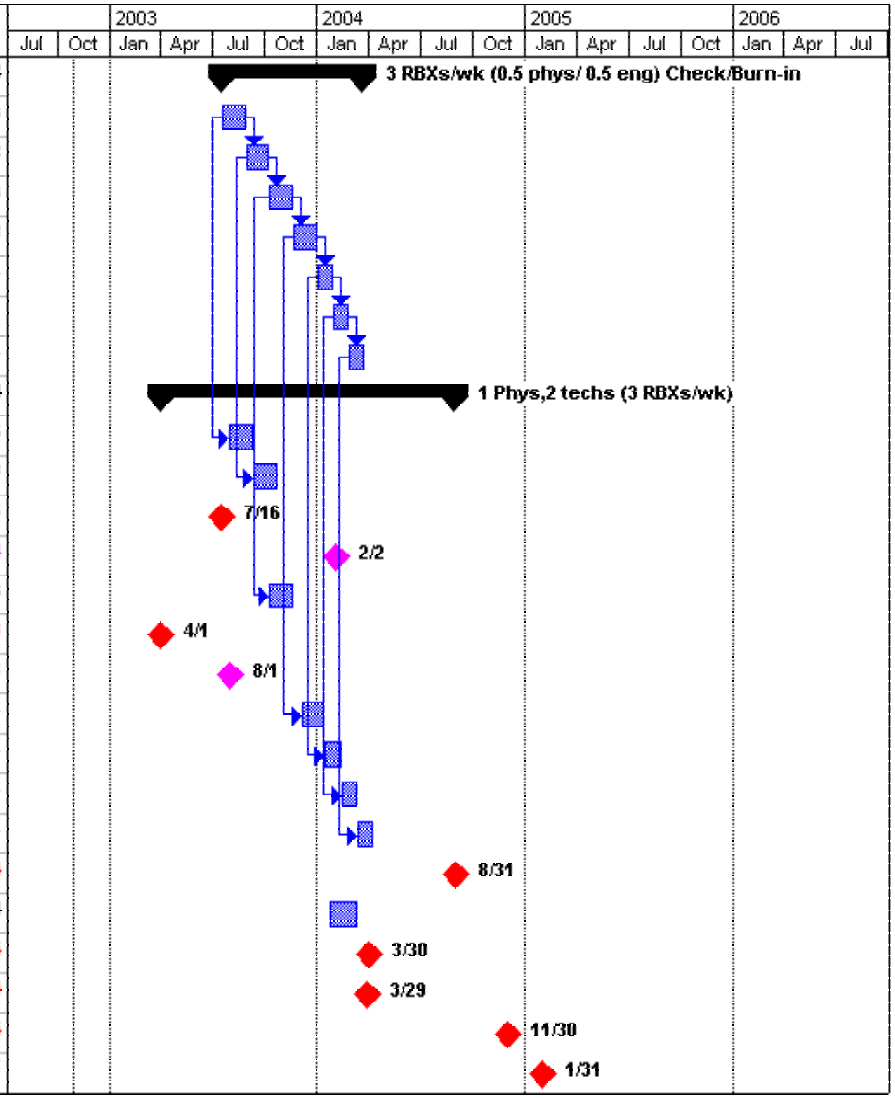
FE Production Schedule

ID	Task Name	Duration	Start	Finish
29	**Test FE Modules (qty 2002)**	**201 days**	**Tue 7/1/03**	**Tue 4/6/04**
30	HE- (qty 234)	23 days	Tue 7/1/03	Thu 7/31/03
31	HB- (qty 234)	23 days	Fri 8/1/03	Tue 9/2/03
32	HE+ (qty 234)	23 days	Wed 9/3/03	Fri 10/3/03
33	HB+ (qty 234)	23 days	Mon 10/6/03	Wed 11/5/03
34	HO 0 (qty 120)	12 days	Thu 11/6/03	Fri 11/21/03
35	HO + (qty 156)	16 days	Mon 11/24/03	Mon 12/15/03
36	HO - (qty 156)	16 days	Tue 12/16/03	Tue 1/6/04
37	HF (qty 300) Probably sooner at BU	30 days	Wed 1/7/04	Tue 2/17/04
38	Spares (qty 334)	35 days	Wed 2/18/04	Tue 4/6/04
39	**HPD Production/Testing (qty 500)**	**362 days**	**Mon 11/4/02**	**Tue 3/23/04**
40	HE- (qty 72)	52 days	Mon 11/4/02	Tue 1/14/03
41	HB- (qty 72)	52 days	Wed 1/15/03	Thu 3/27/03
42	HE+ (qty 72)	52 days	Fri 3/28/03	Mon 6/9/03
43	HB+ (qty 72)	52 days	Tue 6/10/03	Wed 8/20/03
44	HO 0 (qty 36)	26 days	Thu 8/21/03	Thu 9/25/03
45	HO + (qty 48)	35 days	Fri 9/26/03	Thu 11/13/03
46	HO - (qty 48)	35 days	Fri 11/14/03	Thu 1/1/04
47	Spares (qty 80)	58 days	Fri 1/2/04	Tue 3/23/04
48	**Assemble/Test RMs (qty 420)**	**175 days**	**Tue 7/8/03**	**Mon 3/8/04**
49	HE- (qty 72)	30 days	Tue 7/8/03	Mon 8/18/03
50	HB- (qty 72)	30 days	Tue 8/19/03	Mon 9/29/03
51	HE+ (qty 72)	30 days	Tue 9/30/03	Mon 11/10/03
52	HB+ (qty 72)	30 days	Tue 11/11/03	Mon 12/22/03
53	HO 0 (qty 36)	15 days	Tue 12/23/03	Mon 1/12/04
54	HO + (qty 48)	20 days	Tue 1/13/04	Mon 2/9/04
55	HO - (qty 48)	20 days	Tue 2/10/04	Mon 3/8/04



FE Production Schedule

ID	Task Name	Duration	Start	Finish
56	**FNAL RBX Integration (qty 108)**	**180 days**	**Tue 7/15/03**	**Mon 3/22/04**
57	HE- (qty 18)	30 days	Tue 7/15/03	Mon 8/25/03
58	HB- (qty 18)	30 days	Tue 8/26/03	Mon 10/6/03
59	HE+ (qty 18)	30 days	Tue 10/7/03	Mon 11/17/03
60	HB+ (qty 18)	30 days	Tue 11/18/03	Mon 12/29/03
61	HO 0 (qty 12)	20 days	Tue 12/30/03	Mon 1/26/04
62	HO + (qty 12)	20 days	Tue 1/27/04	Mon 2/23/04
63	HO - (qty 12)	20 days	Tue 2/24/04	Mon 3/22/04
64	**Install RBXs on Detector (qty 108)**	**371 days**	**Tue 4/1/03**	**Tue 8/31/04**
65	Install HE- RBXs on Detector (qty 18)	30 days	Tue 7/29/03	Mon 9/8/03
66	Install HB- RBXs on Detector (qty 18)	30 days	Tue 9/9/03	Mon 10/20/03
67	**HB:End Electronics Installation in RBXs**	**1 day**	**Wed 7/16/03**	**Wed 7/16/03**
68	***** Move HB:End Electronics Installation in**	**1 day**	**Mon 2/2/04**	**Mon 2/2/04**
69	Install HE+ RBXs on Detector (qty 18)	30 days	Tue 10/7/03	Mon 11/17/03
70	**HE+1:RBXs ready for Installation**	**1 day**	**Tue 4/1/03**	**Tue 4/1/03**
71	***** MoveHE+1:RBXs ready for installation**	**1 day**	**Fri 8/1/03**	**Fri 8/1/03**
72	Install HB+ RBXs on Detector (qty 18)	30 days	Tue 12/2/03	Mon 1/12/04
73	Install HO 0 RBXs on Detector (qty 12)	20 days	Tue 1/13/04	Mon 2/9/04
74	Install HO + RBXs on Detector (qty 12)	20 days	Tue 2/10/04	Mon 3/8/04
75	Install HO - RBXs on Detector (qty 12)	20 days	Tue 3/9/04	Mon 4/5/04
76	**HO:End Electronics Installation in RBXs**	**1 day**	**Tue 8/31/04**	**Tue 8/31/04**
77	**Install HF Electronics in 3U EuroCrates**	**34 days**	**Wed 1/21/04**	**Mon 3/8/04**
78	**HF Readout Box Installation Complete**	**1 day**	**Tue 3/30/04**	**Tue 3/30/04**
79	**Slice 1 in SX5 Complete**	**1 day**	**Mon 3/29/04**	**Mon 3/29/04**
80	**Slice II in SX5 Complete**	**1 day**	**Tue 11/30/04**	**Tue 11/30/04**
81	**SX5 Magnet Test**	**1 day**	**Mon 1/31/05**	**Mon 1/31/05**



Testing Scenarios

Please Reference HB Schedule

Line 29 - Checkout FE Module

- Checked out with DAQ hardware/software
- Require 10 good cards/day
- 1+ technicians allocated
- All boards, chips 100% tested prior to assembly
- Expect high yield of first time pass >90%
- Technicians will repair all cards which don't pass initial checkout; expect >99% yield

Testing Scenarios

Please Reference HB Schedule

Line 48 – Assemble Readout Module and checkout

- An RM includes three FE cards, an HPD and associated cabling
- Require 12 good RMs/wk
- 3 technicians allocated
- All boards 100% tested prior to assembly
- RMs will be tested/read out by HCAL local DAQ system, hardware will allow for charge injection to test QIEs
- Expect high yield of first time pass >90%
- Technicians will repair RMs which don't pass initial checkout; expect 100% yield

Testing Scenarios

Please Reference HB Schedule

Line 56 – Burn in RBXs

- An RBX receives 4 RM modules
- Boxes are left powered for a week and then re-tested
- 3 RBXs will be completed each week
- ½ physicist, ½ engineer allocated
- RBXs will be tested/read out by HCAL local DAQ system, hardware will allow for charge injection to test QIEs
- Expect high yield of first time pass >95%
- Technicians will repair all RBXs which don't pass initial checkout; expect 100% yield

Testing Scenarios

Please Reference HB Schedule

Lines 64 – Ship RBXs to CERN and Re-test

- RBXs are shipped to CERN,
- Two techs and a physicist will re-test the boxes on receipt and before installation.
- RBXs will be tested/read out by HCAL local DAQ system, hardware will allow for charge injection to test QIEs
- Expect high yield of first time pass >95%
- Technicians will repair any RBXs which don't pass initial checkout; 100% yield

Summary

1. **Front-end electronics are on schedule**
   - Very little schedule float for QIE, GOL, LH4913
   - Infrastructure at SX5 for burn-in and slice tests is of concern
2. **Steady Progress**
   - QIE development/bench studies – begin 1999
   - 2 channel card – June ‘01
   - 2 channel card w/HPD – Aug ‘01
   - 6 channel card w/HPD – March ’02
   - 144 Channels in the test beam – Aug ’02
   - 200 Pre-prod cards will be built Feb/Mar’03

Future Focus

1. Development of a low-noise cable and connector configuration for the HF photomultipliers
2. Board level radiation testing for SEE and SEL
3. Ramping up the nested production, test and assembly lines for readout modules
4. 200 card Pre-production run to be completed early ’03
5. Full Production to start July/Aug. ‘03